REMARKS

Claim amendments

Applicant amends the claims to more clearly recite the function of the second retry determination circuit. In particular, Applicant observes, from the Examiner's remarks, that the word "timing" has been misunderstood.

With respect to the recitation of a timing signal "derived from the recording medium," Applicant draws attention to the use of the pit clock signal, which is derived from observing certain timing pits on a disk.

Applicant also amends language referring to "one or more memories" because a recitation of one memory already covers a structure with two or more memories. Hence, "one or more memories" is redundant.

Section 103 rejection

Prior to their amendment above, independent claims 3 and 7 stood rejected as being rendered obvious by the combination of *Willis*[1] and *Arataki*.[2] With regard to claim 3, the Examiner appears to regard *Willis* as disclosing all claim elements with the exception of the encoder "being configured to receive data from the buffer memory."

***Willis* fails to disclose a synchronization circuit**

In fact, *Willis* also fails to disclose an address memory "configured to store a write-data-address when the *writing* of data to the recording medium is interrupted." This is because in *Willis*, it is *playback* that is interrupted, not *recording*.

Willis describes a system that is intended to solve the following problem: suppose you are watching and recording a television program when suddenly, the telephone rings. If you answer

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[1] *Willis*, U.S. Patent No. 6,693,857.
[2] *Arataki*, U.S. Patent No. 5,931,955.

the telephone, you may miss a crucial moment in the program. If you ignore the telephone, you may miss an important call.

The *Willis* system offers a way out of this difficulty. In the *Willis* system, one presses a pause button to interrupt playback. Meanwhile, *recording continues*. Then, when you have completed the call, you unpause. In response, the *Willis* system then resumes playback from the point at which you paused.[3]

It is clear therefore that in *Willis*, pressing the pause button interrupts *playback*; it does *not* interrupt *recording*. Indeed, the whole point of *Willis* is to avoid interrupting the recording when one interrupts playback.

There is no interruption of *recording* in *Willis*. Not surprisingly, there is also no disclosure of an address memory "configured" to store a write-data-address "when the writing of data to the recording medium is interrupted." After all, if *recording* is not interrupted, there is no reason to configure an address memory as claimed.

The Examiner has not indicated where *Arataki* might supply this deficiency in the teaching of *Willis*. Nor is any such teaching apparent in *Arataki*. Therefore, even if one were to somehow combine *Willis* with *Arataki*, the result would still fail to disclose the synchronizing circuit as claimed.

First and Second Retry Determination Circuits

The Examiner has drawn attention to FIGS. 1 and 3 as somehow disclosing the retry determination circuits.

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[3] *Willis*, col. 6, lines 17-26, ("Such a function can be utilized, for example, when a viewer is watching a television program and is interrupted by a visitor or a phone call. During the time the viewer is unavailable, the recorder continues to record the program. After some period of time...the viewer will want to resume viewing the program from the point at which viewing was interrupted. At this point, the device must start playing back the recording from the beginning of the pause, while continuing to record the incoming program material.").

With regard to FIG. 1, Applicant cannot identify any structure that might reasonably correspond to either of the claimed retry determination circuits. Applicant requests that the Examiner identify precisely what structures in FIG. 1 are regarded as the first and second retry determination circuits.

With regard to FIG. 3, Applicant fails to see any connection between the subject matter of FIG. 3 and the claimed retry determination circuits. According to FIG. 3, pausing playback causes recording to be carried out on odd number tracks. When playback is resumed, as shown in FIG. 8, the even numbered tracks are filled in. This procedure minimizes the distance traveled by the recording head so that it can switch rapidly between recording and playback, thereby giving the viewer the illusion that playback and recording proceed simultaneously. This has nothing to do with the claimed subject matter.

In connection with those figures, the Examiner states

> *"matching address as of a write data and a read data is a process of recording the data into a proper track address which is provided by the encoding means".*[4]

Applicant is unable to understand precisely what the Examiner is trying to say, much less what it has to do with the first and second retry determination circuits. To assist Applicant in better understanding the Examiner's position, Applicant requests that the Examiner quote verbatim from *Willis* that text that is regarded as disclosing the claimed first and second retry determination circuits.

In his remarks in the final office action,[5] the Examiner appears to be suggesting that because data in a buffer has an address, and because data on a disk also has an address, there

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[4] *Final Office Action*, page 5.
[5] *Final Office Action*, page 2.

must be a first retry determination circuit "for determining whether an address of the written data....and the write-data-address...are the same."

It is clear that the Examiner cannot point to a specific structure in *Willis* as corresponding to the first retry determination circuit. Having failed to identify such a structure, the Examiner now asserts that such a structure, even if not disclosed, is inherent because it is inconceivable that reading and writing data can be carried out without a retry determining circuit as claimed.

This is, of course, not the case. For example, in a conventional method of writing data to a disk, the processor passes data stored in a buffer to a disk driver. Then, the disk driver selects an address on the disk and writes the data to that address. In that case, there is both a buffer address and a disk address, but there is no need to determine if the two "are the same."

With regard to the second retry determination circuit, the Examiner appears to suggest that such a circuit is inherent because data that is encoded at one sampling rate must be decoded at the same sampling rate. Therefore, even if no such circuit is disclosed, there must exist a circuit to ensure such compatibility.

Applicant's second retry determination circuit does not inspect sampling rate. Its function is to ensure that writing is restarted only when an appropriate portion of the disk is under the write head. To assist it in carrying out this function, the circuit relies in part on a timing signal that is derived from the recording medium. In the illustrated embodiment, with the recording medium being a disk, the timing signal is derived from pits on the disk, with the passage of pits being indicative of the spin rate of the disk. However, with other kinds of recording media, the timing signal can be encoded in different ways.

It is clear therefore that *Willis* fails to disclose the first and second retry determination circuit. The Examiner has not indicated where *Arataki* might supply this deficiency in the teaching of *Willis*. Nor is any such teaching apparent in *Arataki*. Therefore, even if one were to

somehow combine *Willis* with *Arataki*, the result would still fail to disclose the claimed invention.

Restart Circuit

To support the proposition that *Willis* discloses a restart circuit, the Examiner draws attention to FIGS. 1 and 15.

With regard to FIG. 1, Applicant cannot identify any structure that might reasonably correspond to the claimed restart circuit. Applicant requests that the Examiner identify precisely what structures in FIG. 1 are regarded as the restart circuit.

FIG. 15 discloses a buffer management algorithm. It is unclear why this figure discloses the existence of the claimed restart circuit. Applicant requests that the Examiner draw attention to the particular portion of this figure that allegedly discloses the claimed restart circuit.

In connection with FIGS. 1 and 15, the Examiner states that

> *"writing each pattern on the recording medium with respect to its location requires a restart write process"*

As pointed out above, in *Willis*, only playback is interrupted, not writing. Applicant fails to appreciate why a "restart write" process is required by *Willi*'s. After all, if writing is never interrupted in the first place, there would be no need to restart it. Accordingly, Applicant requests that the Examiner quote verbatim from *Willis* the language that is regarded as disclosing the retry circuit.

It is clear therefore that *Willis* fails to disclose the restart circuit. The Examiner has not indicated where *Arataki* might supply this deficiency in the teaching of *Willis*. Nor is any such teaching apparent in *Arataki*. Therefore, even if one were to somehow combine *Willis* with *Arataki*, the result would still fail to disclose the claimed invention.

Summary

Now pending in this application are claims 3-10, of which claims 3 and 7 are independent. Applicant encloses an RCE fee. A notice of appeal was filed on November 18, 2005. Accordingly, Applicant encloses a petition to extend the response period from January 18, 2006 up to an including March 18, 2006. No additional fees are believed to be due in connection with the filing of this RCE. However, to the extent fees are due, or if a refund is forthcoming, please adjust our deposit account 06-1050, referencing attorney docket "10449-033001."

Respectfully submitted,

Date: *March 17, 2006*

/Faustino A. Lichauco, Reg. 41,942/
Faustino A. Lichauco
Reg. No. 41,942

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

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